

Short reasons for long vectors in HPC CPUs: a study based on RISC-V

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ABSTRACT

For years, SIMD/vector units have enhanced the capabilities of modern CPUs in High-Performance Computing (HPC) and mobile technology. Typical commercially-available SIMD units process up to 8 double-precision elements with one instruction. The optimal vector width and its impact on CPU throughput due to memory latency and bandwidth remain challenging research areas. This study examines the behavior of four computational kernels on a RISC-V core connected to a customizable vector unit, capable of operating up to 256 double precision elements per instruction. The four codes have been purposefully selected to represent non-dense workloads: SpMV, BFS, PageRank, FFT. The experimental setup allows us to measure their performance while varying the vector length, the memory latency, and bandwidth. Our results not only show that larger vector lengths allow for better tolerance of limitations in the memory subsystem but also offer hope to code developers beyond dense linear algebra.

KEYWORDS

RISC-V, HPC prototypes, vector computing, SIMD, memory bandwidth, memory latency

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1 INTRODUCTION AND RELATED WORK

Various approaches to vector computing exist, with the prevalent “classical” Single Instruction, Multiple Data (SIMD) method employed by x86 architectures. Recently, two pivotal technological

developments have driven the progression of research and software advancement within the realm of vector computing: the Arm Scalable Vector Extension (SVE) and the NEC Aurora SX architecture. Arm’s innovation introduces a more adaptable and sophisticated approach to vectorizing code, supporting vector lengths of up to 32 double precision elements, with a register size of 2 kbits, as detailed by Rico et al. in [9]. On the other hand, the NEC Aurora SX takes an even more radical design stance, presenting a CPU equipped with vector registers accommodating a staggering 256 double precision elements, spanning 16 kbits, as elaborated by Takahashi et al. in [10].

These advancements raise significant inquiries concerning vector architectures, as explored by Ishii et al. in [3]. Key among these are inquiries into the optimal vector length, the ideal vector register size, and the most favorable memory performance metrics, encompassing both bandwidth and latency, that should complement a vector architecture. Beyond the purely architectural questions, the intricacies of simulating and benchmarking vector architectures also come to the fore, as expounded upon by Ramirez et al. in [8].

Indeed, diverse scientific communities are now intently investigating the potential of long-vector computing as a means to speedup their computational endeavors. Importantly, these pursuits often extend beyond the confines of classical high-performance computing (HPC) operations, as demonstrated e.g., by Valassi et al. in [11] and by Diehl et al. in [1]. In our study, we embark on the task of quantifying the precise influence of vector length, memory bandwidth, and memory latency on distinct code implementations. Our objective is to substantiate the claim that vector architectures, particularly those leveraging extended vectors, offer robust solutions for gaining performance while tolerating memory latency and memory bandwidth.

Additionally, since our analysis delves into kernels characterized by non-dense computations, we endeavor to convey a broader message: the realm of scientific software encompasses domains beyond those rooted in dense linear algebra and vector architectures offer hope to all scientific application developers.

Lee et al., in [5] present an overview of the RISC-V technologies leveraging the RISC-V Vector Extension available from the industry and the academia. For the evaluation part of our work, we have chosen to focus on the hardware development of a RISC-V-based design that targets the HPC domain and is developed within the

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European Processor Initiative project. The system leverages a RISC-V core coupled with a Vector Processing Unit implementing the RISC-V Vector Extension RVV-v0.7.1 and it allows to configure Vector Length (VL) and memory parameters.

The main contributions of this paper are: *i)* we present a flexible FPGA-based setup (Software Development Vehicle) including a RISC-V core connected to a configurable VPU on which we can co-design hardware and software in a flexible and fast way; *ii)* we quantify the effects of VL, memory latency, and memory bandwidth on a real RISC-V CPU implemented on FPGA; *iii)* we study four different kernels that are not-dense: SpMV, BFS, PR and FFT.

The rest of this paper is structured as follows: Section 2 presents the experimental setup on which we performed the measurements presented in this paper. Section 3 explains the methodology adopted, the software setup and the codes selected for the benchmarking. In Section 4 we provide details about the evaluation, reporting performance measurements when varying VL, memory latency and memory bandwidth. We conclude the paper with our findings and comments in Section 5.

2 EXPERIMENTAL SETUP

In this section we describe our experimental setup called FPGA Software Development Vehicle (FPGA-SDV), which is developed within the European Processor Initiative (EPI) project¹ and emulates parts of the EPI European Accelerator (EPAC) design. The parts of EPAC that we emulate on the FPGA design include:

- Atrevido, a RISC-V super-scalar core developed by SemiDynamics².
- Vitruvius Vector Processing Unit (VPU) [7] developed by BSC³, which is tightly coupled to the core, contains eight lanes and is capable of operating on vectors of 256 double-precision elements (i.e., 16384-bit wide vector registers). Each lane includes a Floating Point Unit (FPU) developed by the University of Zagreb [4].
- Network on Chip (NoC) with 2D Mesh topology developed by EXTOLL⁴.
- Shared L2 Cache developed by FORTH-ICS⁵ which is tightly coupled with a MESI-based coherence Home Node developed by Chalmers⁶, collectively called L2HN.

Figure 1 provides a simplified block diagram of each components of FPGA-SDV: Atrevido in red, VPU+FPU in blue, NoC in yellow and L2HN in purple.

Our setup comprises of a Virtex UltraScale+ HBM VCU128 PCIe FPGA board⁷ and a AMD Ryzen5 5600 host server with 32 GB of DDR4-3200 memory, both mounted on a Mini-ITX motherboard. The server runs Ubuntu Server Linux 20.04 with local storage and a mounted Network Filesystem. The VCU128 board includes a VU37P FPGA device with 8 GB of integrated HBM memory and 4.5 GB of external DDR4 memory. Figure 2 shows the connectivity between the host server and the VCU128 board.

¹European Processor Initiative. <https://www.european-processor-initiative.eu/>

²SemiDynamics. <https://semidynamics.com/>

³Barcelona Supercomputing Center. <https://bsc.es/>

⁴EXTOLL. <http://extoll.de/>

⁵FORTH-ICS CARV. <https://www.ics.forth.gr/carv>

⁶Chalmers University. <https://www.chalmers.se/en/departments/cse/>

⁷Xilinx VCU128. <https://www.xilinx.com/products/boards-and-kits/vcu128.html>

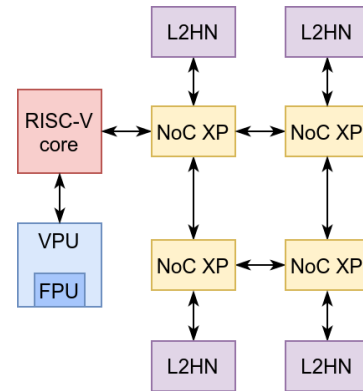


Figure 1: Simplified architecture of the FPGA-SDV

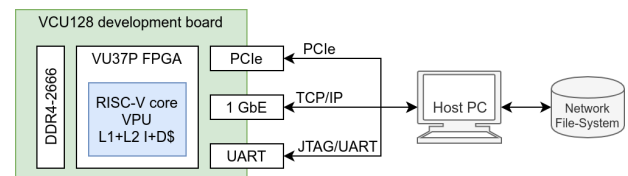


Figure 2: Connection between host server and VCU128 board: schematic view

In this work we emulate on the FPGA one instance of Atrevido with VPU and four instances of L2HN connected via a 2×2 Mesh NoC. The host server communicates with the VCU128 primarily through PCIe Gen3 x16, 1 Gbit Ethernet, and other low-speed interfaces like JTAG and UART. A typical scenario for experimenting with the FPGA-SDV includes the following steps:

- Use the host to program the VCU128 bitstream with the emulated system via JTAG.
- Use the host PCIe interface to load Linux images into the VCU128 DDR4 memory, perform any additional register configurations like modifying the memory latency as described in Section 2.2, and initiate boot on the emulated system.
- Access the emulated system's Linux terminal via UART or SSH via Ethernet.
- Mount a Network Filesystem (NFS) via Ethernet in order to share files between the host and the emulated system, run benchmarks, and perform tests.

2.1 Variable Vector Length

The RISC-V Vector Extension⁸ has some characteristics that differentiate it from other vector extensions, such as Intel's AVX or ARM Neon. The VL is not constrained by the Instruction Set Architecture (ISA); it is implementation-specific like ARM's SVE extension. Additionally, the VL can change on runtime. A code can execute some instructions with a given VL and some other instructions with a shorter or longer VL, which means that the architecture adapts to the codes seamlessly without predicates or loop prologues/epilogues. This also allows the compiler to generate VL-agnostic code,

⁸RISC-V "V" Extension. <https://github.com/riscv/riscv-v-spec/blob/master/v-spec.adoc>

meaning that the binaries do not need to know the machine’s maximum implemented VL, thus enabling portability.

Inside the core we can find a custom Control and Status Register (CSR) that contains the maximum VL of the machine. Usually this value would be hard-coded in the hardware, but having it in a CSR lets us programmatically modify it with lower values to run interesting experiments. Lowering the VL may degrade performance, but allows us to quantify its effect and see how it interacts with other parameters of the core.

2.2 Latency Controller

The Latency Controller is a hardware module which can artificially introduce additional latency to the DDR4 memory subsystem. In our experimental setup the FPGA emulated Atrévido + VPU + NoC + 2 × 2 L2HN system runs at a lower frequency compared to DDR4 of the VCU128 FPGA, i.e., 50 MHz compared to 333 MHz. Therefore, from the emulated system’s perspective the memory requests appear to complete with lower latency compared to a typical production system; the minimum memory access latency observed in the FPGA emulated system at 50 MHz is approximately 50 clock cycles. Thus, this module primarily serves two goals: (a) to emulate the memory latency of a typical system and (b) evaluate how latency affects the behavior and performance of benchmarks running on the emulated system. Practically, the Latency Controller offers two functionalities: (a) stalls reads and writes to DDR4 memory for a user-defined number of clock cycles in a pipelined fashion, (b) provides a software configurable interface so that users can modify the memory latency in a programmable and dynamic way on the emulated system without re-configuring the FPGA.

2.3 Bandwidth Limiter

The Bandwidth Limiter is a hardware module that can throttle the bandwidth of the DDR4 memory subsystem. More specifically, this module operates in time windows and permits only a limited number of memory requests per time window. For example, to throttle the bandwidth at 33% of the peak only two registers need to be set: the value of the numerator to 1 and the value of the denominator to 3 to achieve the fraction 1/3. Then, the module allows only 1 memory request to be issued per time window, which is 3 clock cycles. The Bandwidth Limiter operates similarly to the Latency Controller and provides the same software configurable interface for flexibility, so that users can experiment with different bandwidth rates quickly without re-configuring the FPGA.

3 METHODOLOGY

The core inside the FPGA runs a regular Ubuntu Server 20.04 with local storage and a mounted Network Filesystem. We compile our codes using an LLVM-based compiler developed at the BSC⁹, which can vectorize for RISC-V using either automatic vectorization or manual vectorization via intrinsics or builtins. The codes we evaluate have been vectorized using a combination of both methods; we use automatic vectorization for short or simple regions of code and intrinsics to perform fine-grained optimizations.

⁹<https://repo.hca.bsc.es/gitlab/rferrer/llvm-epi>

3.1 Codes Selected for the Evaluation

We employ four computationally relevant codes in our evaluation. All of them are vectorized for RISC-V using the LLVM-based compiler with vectorization support.

First, we use a vectorized Sparse matrix-vector multiplication (SPMV) targeting long-vector architectures [2]. The C sources can be accessed upon request in BSC repositories¹⁰. The input used for this evaluation is the “CAGE10” matrix¹¹. SPMV is a relevant code in High-Performance Computing (HPC) because it behaves more similarly to real scientific applications than artificial benchmarks due to its use of sparse data structures and being memory bound. It is normally used to highlight the efficiency of the memory subsystem of an architecture.

Secondly, we use long-vector implementations of two graph algorithms, Breadth-First Search (BFS) and Page-Rank (PR) [13]. The C++ sources can also be accessed upon request¹². Graph algorithms are a relevant HPC topic in various fields like networks, infrastructure, social circles, or internet webpages. BFS is one of the best-known examples and a building block of many other algorithms. PR presents slightly more computational intensity, and it is used to assign scores to nodes in a graph. Web browsers such as Google use it to determine a webpage’s relevance. Both codes used a graph of 2^{15} nodes for the evaluation.

Finally, we use a vectorized implementation of the Fast Fourier Transform (FFT) kernel [12]. The C sources can be accessed upon request¹³. For the evaluation, we selected an FFT size of 2048 elements. The FFT is a relevant code because it presents both arithmetic intensity and complex memory access patterns, which makes it a challenge for vector architectures. It is also used as a building block in many scientific codes including signal or image processing, numerical analysis, genomics, or astronomy.

3.2 Tools Used for Measurements

To obtain fine-grained measurements and mitigate OS noise, we read the hardware counter that counts CPU cycles. We then calculate the average of these measurements over five runs. As the variation among the runs is below 3%, we have chosen to exclude error bars to prevent unnecessary cluttering of the plots.

4 EVALUATION

In this section, we evaluate the behavior of the four codes when we artificially introduce latency, throttle bandwidth, or alter the maximum VL of our system. The analysis of vector architectures often revolves around the benefit of operating many data elements simultaneously, without giving much regard to their interaction with the memory. Using long vectors, we can pack hundreds of memory requests in a single instruction, thus dramatically reducing the number of times we pay the latency to the memory, while also highly utilizing the bandwidth since each transaction is moving many more data elements compared to scalar accesses.

¹⁰<https://repo.hca.bsc.es/gitlab/cgomez/spmv-long-vector>

¹¹<https://sparse.tamu.edu/vanHeukelum/cage10>

¹²<https://repo.hca.bsc.es/gitlab/pvizcaino/graph-v>

¹³<https://repo.hca.bsc.es/gitlab/pvizcaino/fft>

4.1 Adding latency

Using the tools described in Section 2.2, we can add an arbitrary number of cycles to the latency between the L2 cache and the main memory. This way, we can simulate a system with more congestion (e.g., with more cores) or with a longer path to the memory and study its effects on scalar and vectorized applications.

With these tests, we aim to showcase that long-vector architectures are more resistant to memory latency than traditional scalar machines. For each code, we study both the scalar and vector implementations. For the vector ones, we also modify the maximum VL of the system in order to study its relation with the latency.

Figure 3 contains four plots with the measured execution time for each of the codes on the y -axis. The x -axis report the extra latency cycles that have been added by the Latency Controller described in Section 2.2. Each plot shows the scalar implementation in blue, and the vector runs with increasing VL in a red gradient: the larger the VL the darker the red. The values of VL considered are expressed in units of double-precision elements: i.e., VL=8 means vector register width of 512 bits (light red) while VL=256 means vector register width of 16 kbits (dark red). This color pattern applied to the VL is maintained for the rest of the document for an easier comparison of the plots.

As anticipated, all the plots in Figure 3 demonstrate an increase in execution time with the addition of extra latency. However, Figure 3 also distinctly illustrates the substantial advantage that the vector code gains from a higher VL. When examining the slopes of the data series, it is evident that as we decrease the VL, the slopes become steeper. This implies that the scalar and low VL implementations are more adversely impacted (i.e., perform worse) by the introduced latency, causing their performance to degrade more rapidly compared to executions with larger VL values.

We propose an alternative data visualization to better study the effect of the VL on the latency resistance in Figure 4. We show one table per each code, with the different implementations (scalar and with different VL values) as columns and the extra latency cycles as rows. The values in each cell of the tables are the execution times normalized against each implementation's run with no additional latency. This way, for each implementation, we show how many times slower they run depending on the extra latency added. In each table we color-code this slowdown from green for the best case (lowest slowdown) to red for the worst case (highest slowdown).

Looking at the tables row by row, we can see that as we add latency, the tables turn red as the slowdown increases. The key observation is that for any added latency row, the slowdown diminishes when we increase the VL, with the minimum slowdown at the right-most column.

Using the SPMV as an example, adding 32 cycles of latency the scalar code runs 1.22 \times slower, while the vector implementation with $vl = 256$ only runs 1.05 \times slower. This is even more pronounced when adding 1024 cycles of latency, with a slowdown of 8.78 \times compared to 3.39 \times .

4.2 Limiting bandwidth

The second use of the tools from Section 2.3 is limiting the bandwidth, from 64 Bytes per cycle downwards. This lets us study how vectors use the bandwidth provided by the system.

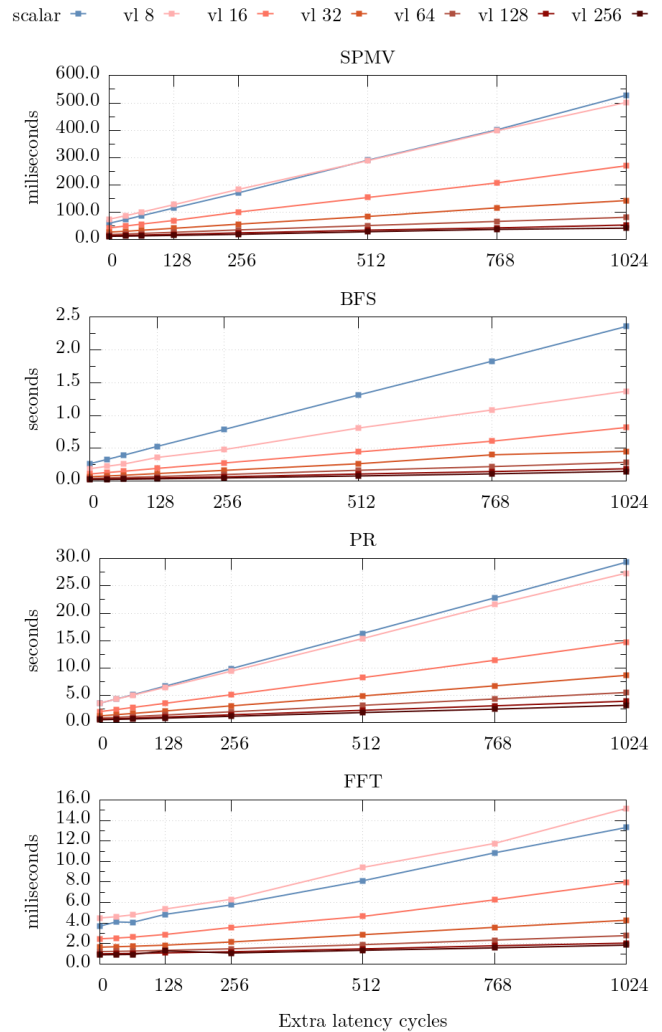


Figure 3: Execution time of the four evaluated codes depending on the added latency, with blue series for scalar implementations and a red gradient series for vector implementations with increasing VL

A scalar architecture normally needs many CPUs sending requests to the memory to fully saturate the bandwidth that the system can provide. On the other hand, long vectors can reach this saturation quicker using only one core, making a more efficient use of the system with a lower number of cores.

Figure 5 shows the same four codes as before, once again with a blue series for the scalar implementation and a red gradient of series for the vector implementations with increasing VL values. The x -axis represents the maximum bandwidth we limit with our Bandwidth Limiter tool. The values of the x -axis are expressed in Bytes per cycles, ranging from 1 to 64 Bytes per cycles in steps of power of 2. The y -axis is the execution time normalized against the same run with a maximum bandwidth of 1 Byte per cycle. This means that lower values on the y -axis are preferred since they represent a shorter execution time.

SPMV (slowdown: time normalized to 0 extra latency)							
Extra latency	0	1.00	1.00	1.00	1.00	1.00	1.00
	32	1.22	1.17	1.15	1.10	1.10	1.07
	64	1.45	1.35	1.32	1.24	1.20	1.13
	128	1.92	1.71	1.63	1.50	1.42	1.29
	256	2.85	2.46	2.34	2.05	1.88	1.67
	512	4.83	3.86	3.57	3.06	2.72	2.33
	768	6.68	5.32	4.81	4.20	3.52	2.90
	1024	8.78	6.70	6.26	5.16	4.32	3.39
		scalar	vl-8	vl-16	vl-32	vl-64	vl-128
			vl-256				

BFS (slowdown: time normalized to 0 extra latency)							
Extra latency	0	1.00	1.00	1.00	1.00	1.00	1.00
	32	1.23	1.19	1.20	1.17	1.12	1.08
	64	1.47	1.37	1.37	1.33	1.32	1.27
	128	1.98	1.90	1.78	1.72	1.65	1.59
	256	2.94	2.53	2.53	2.44	2.38	2.19
	512	4.90	4.27	4.06	3.94	3.89	3.59
	768	6.83	5.72	5.56	5.97	5.20	4.84
	1024	8.80	7.23	7.47	6.76	6.73	6.24
		scalar	vl-8	vl-16	vl-32	vl-64	vl-128
			vl-256				

PR (slowdown: time normalized to 0 extra latency)							
Extra latency	0	1.00	1.00	1.00	1.00	1.00	1.00
	32	1.22	1.20	1.18	1.19	1.17	1.15
	64	1.44	1.40	1.38	1.37	1.34	1.32
	128	1.89	1.81	1.76	1.75	1.69	1.64
	256	2.79	2.63	2.53	2.50	2.40	2.30
	512	4.61	4.30	4.09	3.99	3.83	3.62
	768	6.44	6.04	5.66	5.48	5.22	4.95
	1024	8.28	7.65	7.31	7.05	6.67	6.30
		scalar	vl-8	vl-16	vl-32	vl-64	vl-128
			vl-256				

FFT (slowdown: time normalized to 0 extra latency)							
Extra latency	0	1.00	1.00	1.00	1.00	1.00	1.00
	32	1.11	1.03	1.03	1.02	1.02	1.01
	64	1.10	1.07	1.06	1.05	1.04	1.04
	128	1.31	1.20	1.17	1.12	1.09	1.09
	256	1.56	1.49	1.44	1.31	1.22	1.20
	512	2.20	2.23	1.88	1.74	1.56	1.47
	768	2.93	2.78	2.54	2.17	1.92	1.78
	1024	3.60	3.59	3.23	2.59	2.28	2.03
		scalar	vl-8	vl-16	vl-32	vl-64	vl-128
			vl-256				

Figure 4: Execution time of the four evaluated codes normalized to their run with 0 extra latency for each implementation. The color gradient goes from minimum slowdown (green) to maximum slowdown (red) for each table

The plots on Figure 5 showcase that the scalar versions do not take advantage of bandwidths higher than 1 or 2 Bytes/Cycle. This is seen as the time curve from the scalar implementations (blue) flattening and creating a plateau at those values. The vector code with $vl = 8$ behaves similarly to the scalar code, taking little advantage of bandwidths higher than 2 or 4 Bytes/Cycles. On the other hand, as we increase the maximum VL of the machine (darker series in the plots), the plateau of the execution time is reached with higher bandwidth values. This implies that codes with larger VL benefit more from having a system with higher bandwidth. In other words, Figure 5 shows that a single core with a vector unit supporting larger VL takes more benefits from being connected to a memory subsystem with higher bandwidth than a scalar core (or a core with shorter VL).

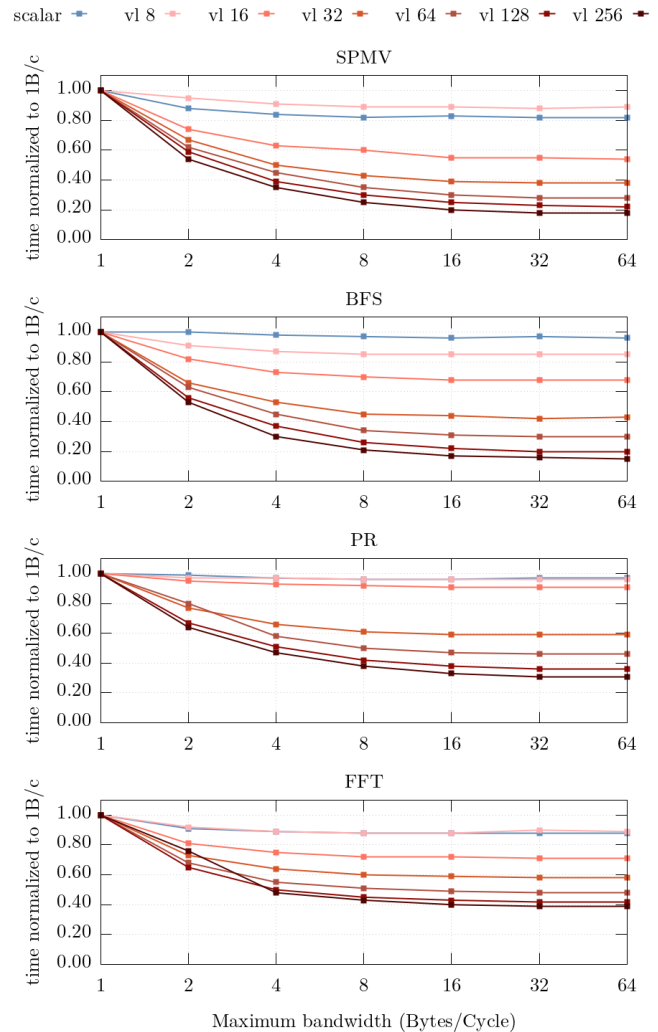


Figure 5: Execution time of the four codes depending on the limited bandwidth, normalized to the run with a limit of 1 Byte/Cycle per each implementation

5 CONCLUSIONS

In this paper we presented an FPGA setup, called FPGA-SDV implementing a scalar RISC-V core coupled with a configurable vector unit with 8 lanes able to process vector of up to 256 double precision elements (16 kbits). The setup is configured so that a user can configure the maximum vector length (applying values from 8 up to 256 double-precision elements), the memory bandwidth (with values from 1 to 64 Bytes per cycle), and the memory latency (adding an arbitrary number of extra-cycles of latency for accessing the main memory).

We used this setup to evaluate four kernels that are relevant in HPC but are not strictly related to dense-algebraic workflow: we considered SPMV, BFS, PR, and FFT.

On those non-dense codes, we showcase two often overlooked benefits of long vector architectures: *i)* tolerate memory latency; *ii)* taking advantage of higher memory bandwidths with a single core;

We highlight the potential of the FPGA-SDV methodology to prove these benefits. The flexibility of our system lets us easily tweak architectural parameters on real hardware, such as the maximum vector length, the bandwidth of the system, or the latency to the main memory. Coupling these features with the methodology described in our previous paper [6] allow us to study HPC-relevant codes and to implement a co-design cycle that provides valuable insights to scientists developers, compiler/system software developers, and hardware architects.

When we degrade the performance of the codes by adding extra memory latency to our system, we observed that the vectorized implementations are less impaired than the scalar ones. This difference is accentuated when the vector implementations use a large vector length, thus showing that long vectors are more resistant to high latencies. In our experimental setup, we also observed that while the single core scalar implementations do not benefit from a bandwidth higher than 1 or 2 Bytes/Cycle, the long vector implementations can naturally use bandwidths of 32 or 64 Bytes/Cycle.

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