

Overview of the RISER Project

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Call: Open source for cloud-based services, GA Nr: 101092993 (HaDEA)



European Commission Horizon Europe 2021-2027

RISER will develop the first all-European RISC-V cloud server infrastructure, significantly enhancing Europe's open strategic autonomy.

- <u>Develop & validate open-source designs for standardized</u>
 <u>form-factor system platforms</u>
 - PCIe Acceleration Card, Microserver (Blade)
 - Use cases: acceleration, networked storage, containerized execution
- Enabling the path towards a <u>European-based cloud infrastructure</u>
 - The first Cloud architecture using RISC-V processor technology being developed within the EPI and EUPILOT projects
 - Key technologies:
 - RISC-V processors, PCI-Express/CXL, Cache-coherent Chip-to-Chip links
- Open hardware interfaces
 - Expand the interface possibilities of EPI/EUPILOT processors:
 - High-speed networking and storage capabilities
 - Essential support for cloud applications and services deployment



RISC-V for Cloud Services - Workshop at RISC-V Summit Europe: June 9, 2023 - Barcelona



Integrated all-European Hardware and Open-Source Software for Cloud Services and Applications

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The Heilmeier Catechism [https://www.darpa.mil/work-with-us/heilmeier-catechism]

- What are you trying to do?
 - Cloud servers based on open ISA and interfaces
- How is it done today, and what are the limits of current practice?
 - x86 servers, proprietary ISA and interfaces
- What is new in your approach and why do you think it will be successful?
 - RISC-V open standards, reuse/repackaging/evolution of results from ongoing related projects (EPI, EUPILOT)
- Who cares?
 - Global applicability in a growing market where cost effectiveness coupled with flexible integration is key
- What are the risks?
 - Execution risk due to technical/organizational complexity, schedule risk due to "upstream" dependencies
- How much will it cost?
 - 656 person-months
- How long will it take?
 - 36 months for "first light"
- What are the mid-term and final "exams" to check for success?
 - Open-access programme for evaluation, deployment in IaaS infrastructure, open-source release of interfaces (HW + SW)

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Can become the **linchpin** in a longer-term roadmap that spans projects

Wiser Server motherboard (example)



Are we there yet with RISC-V?

Firmware:

UEFI

ACPI

SMBIOS

+ onboard devices

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(hint: attend the panel)

+ setup of memory controllers + I/O device controllers

Horizon Europe 2021-2027 O SAS3808 (-GC only) LSEDS2 6.0 PM CODE BAR CODE Supermicro X13SET-G

