

# RISC-V<sup>®</sup>

*Everywhere*

The Road Ahead  
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# Overview

- RISC-V Overview
- Why People Use RISC-V
- RT-Thread & RISC-V
- Portability
- Embedded & Real Time ISA Extensions
- SW ecosystem

# The definition of open computing is RISC-V

**RISC-V is the most prolific  
and open Instruction Set  
Architecture in history**

- RISC-V is inevitable
- RISC-V enables the best processors
- RISC-V is rapidly building the strongest ecosystem

10s of Billions of RISC-V cores  
deployed for profit!

# Open Source HW or Open Standard?

- We are officially an Open Standard HW ISA Architecture
- We are an Open Standard that works heavily with Open Source upstream projects (LINUX, GCC, LLVM, etc.)
- We don't do reference implementations
- Our work product are specifications with support from Golden Models and Basic Tests

# Unlike Open Source Software ...

- Proprietary Custom Extensions are Encouraged and Welcome
- Products don't just include the ISA, they can do custom implementations/extensions of/to the ISA
- Copyleft is a non-sequitur
- No restrictions on how the specification can be used
  - Only restrictions on branding

# Why RISC-V?

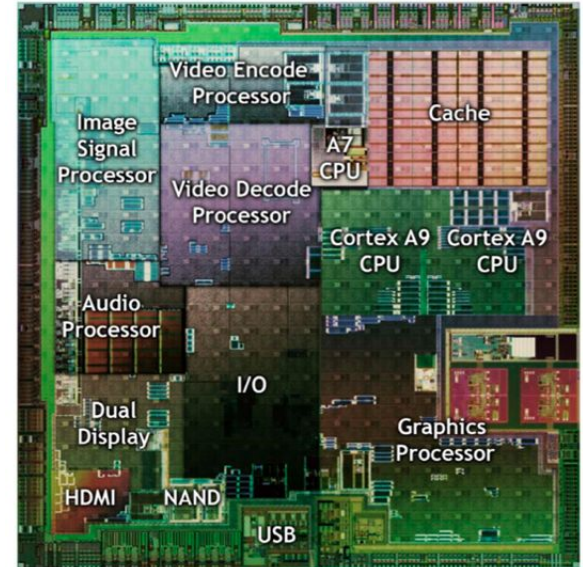
- Flexibility
- Cost
- Ecosystem
- Our position in History
- EDA Renaissance
- Pride of Ownership

# SoC ISA Balkanization

- Applications processor (usually ARM)
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- **> dozen ISAs on some SoCs - each with unique software stack**

## Why?

- Apps ISA too big&inflexible, poor base for other cores
- Apps ISA proprietary, cannot be used by others' IP
- IP bought from different places, each proprietary ISA
- Engineers build home-grown ISA cores (don't do this!)



NVIDIA Tegra SoC



# RISC-V SOC Opportunities

- Move all cores on SoC to RISC-V-based cores
  - Applications processors
  - Graphics processors
  - Image processors
  - AI/ML accelerators
  - Radio DSPs
  - Audio DSPs
  - Security processors
  - Power-management processors

# Fragmentation versus Diversity



## **Fragmentation:**

Same thing done different ways



## **Diversity:**

Solving different problems



# How is RISC-V Avoiding Fragmentation?

Two powerful forces keep fragmentation at bay:

- **Users:** No one wants a repeat of vendor lock-in.
- **Software:** No one, not even nation state, can afford their own software stack. Upstream open-source projects only accept frozen/ratified Foundation standards.

# Portability

- **Unified common standard and a robust Software Ecosystem**
- **A robust economy around systems and software is reliant on portability**
- Application & Runtime Software
  - Profiles
  - API (e.g. POSIX)
- Operation Systems
  - Platforms
  - Supervisor Execution Environment (SEE)
  - Profiles

# Profiles

- Generational groups of instructions that work together and present a unified target for the software ecosystem
- Always include a base (a base are a group of state, instructions and behaviors fundamental to being RISC-V)
- Optionally include one or more extensions (like bases, extensions are a group of state, instructions, and behaviors). Extensions may be mandatory, optional, or non-profile options (n/a)
- Major and minor releases. We use Major releases to be targets for the SW ecosystem. Minor releases are checkpoints
- Initial implementations of profiles are likely available from members 12-48 months after a profile is ratified
- Current profiles (RVA) all targeted at RICHOS, General Purpose Multi-User computing. More to come.
- Profiles can live and be used forever. The implementers decide on adoption and lifetime

# Managing Diversity

## Raw extensions

- Base + standard extensions + custom extensions
- Full suite of options available for experimentation and specialized uses
- Massive combinatorial space of options

## ISA Profiles

- Packages of ISA extensions for given domain
- Initial set: RVI20 (basic), RVA20/22/23 (application processor)
- Factor out common ISA combinations for use in platform standards

## Platform standards

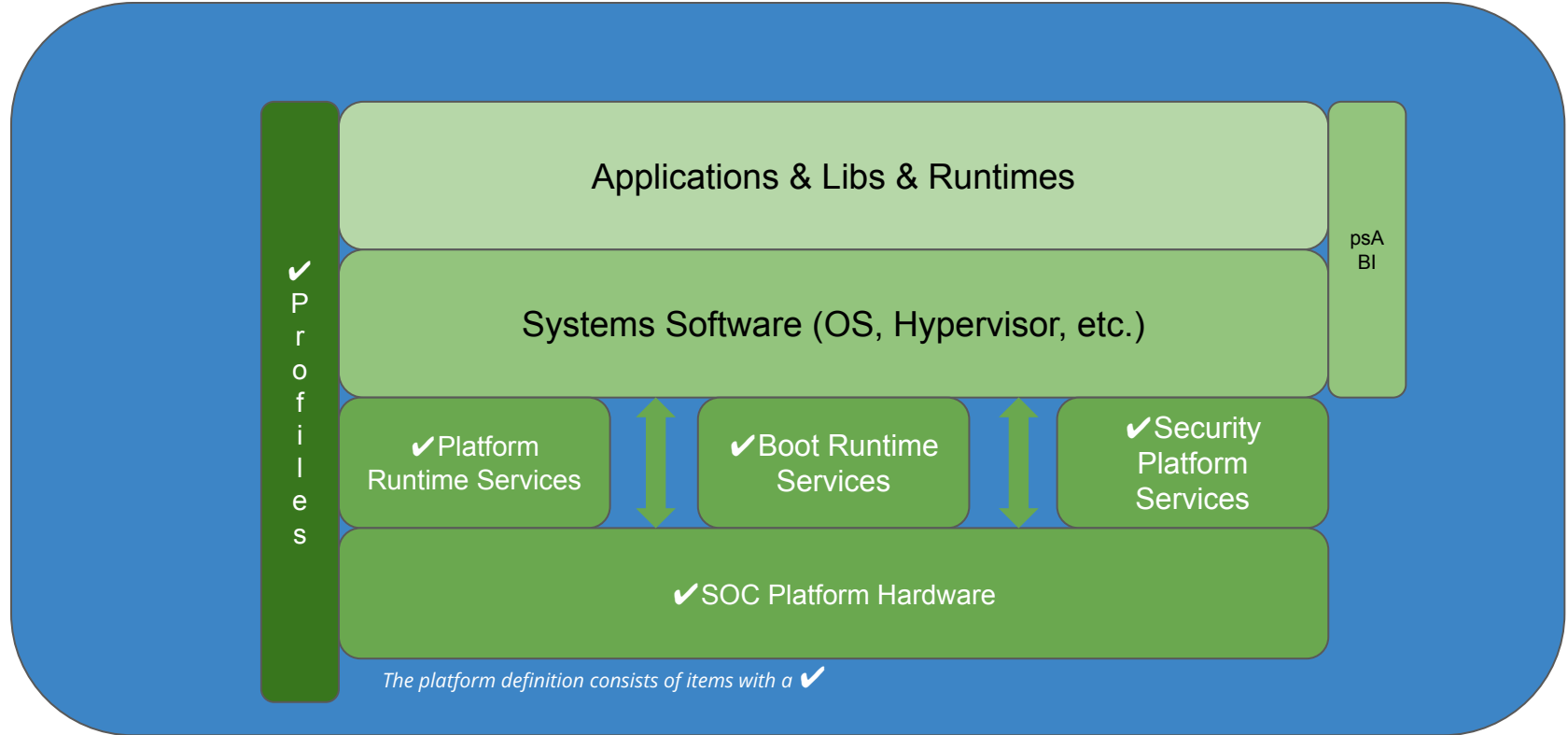
- Hardware/software standards for platforms (much more than just ISA)
- Initial focus OS-A platform for Unix-like OS (includes IOMMU, AIA, etc)

# Profiles

Bases	Public Name 1			Name 2		Future
RV32I RV64I	RVI[20] <i>RVI20U32</i> <i>RVI20U64</i> RV32I RV64I	RVA20 <i>RVA20U64</i> <i>RVA20S64</i> RV64I	RVA22 <i>RVA22U64</i> <i>RVA22S64</i> RV64I	RVA23  RV64I		
Load Store Jumps Branches Add Subtract Logical	On years released, this only has a Mandatory Base  <i>All other compatible ratified extensions are optional</i>	Mul/Div Atomics Compressed Float Double Priv 1.11 MemRegions Fences VirtualMem	Vector Bitmanip Scalar Crypto FP16 Priv 1.12 Hypervisor Cache	Vector Crypto PtrMasking BFloat16 Zcompressed Priv 1.13	Android Features	More profile types: RVB, RVM RV128 Matrix Ops SPMP/IOPMP CFI CHERI GPU 48/64 bit instructions
	MAJOR			MAJOR		

- Only a subset of extensions are listed above and it is not an exhaustive list
- Some extensions may be optional or non-profile in one profile and be mandatory in another

# Platforms





# ISA Extensions Targeted at Embedded and Real Time

- Extensions: Fast Interrupts, Compressed Instructions (plus Zc\*), FP in integer registers, Multiply without divide, Vector for embedded, S mode timer access, S mode w/o MMU, Wait on reservation set, Pause Hint, Physical Memory Protection, Scalar Crypto
- Profile Families: RVI, RVB, RVM
- Bases: RV32I, RV32E, RV64E

# What We Have Done This Year

- Ratified ISA Specifications
  - Profiles, Code Size Reduction
- Ratified Fast Tracks
  - Counters, Total Store Ordering, RV32E/RV64E, Non Temporal Hints
- Documentation
  - Unpriv in AsciiDoc, AsciiDoc Priv draft
- New Task Groups & Special Interest Groups
  - Debug, Trace, and Performance Monitoring (DTPM) TG , Graphics SIG, RISC-V Common Software Interface (RVM-CSI) SIG, Vector (SIMD) SIG, Control Transfer Records TG

# What's Coming Soon?

- Profiles
  - RVA23, RVI23, RVB23, RVM23, BOD committee on comprehensive ACTs & Certification
- Platforms
  - Portability for Systems Software (PRS, BRS, Platform Security, SOC HW, Profiles)
- ISA
  - Advanced Interrupts, QOS Register Interface, Control Transfer Records, Debug, Fast Interrupts, I/D Synch, Priv 1.13, Shadow Stacks/Landing Pads, Vector Crypto, Vector FP16
- ISA Fast Tracks
  - CAS, BFloat16, Conditional Ops, Counter Mode Filtering, HW PTE A/D, Maybe Ops, Additional Scalar FP, Counter Delegation,
- Non-ISA
  - IOMMU, Confidential VM extension, IOPMP, Nexus Trace,
- Documentation
  - Full time RVI DOC Architect/Writer approved
  - BOD committee on dev experience (content & UX)
  - Glossary, Navigation

# Software Ecosystem

This is our number one priority

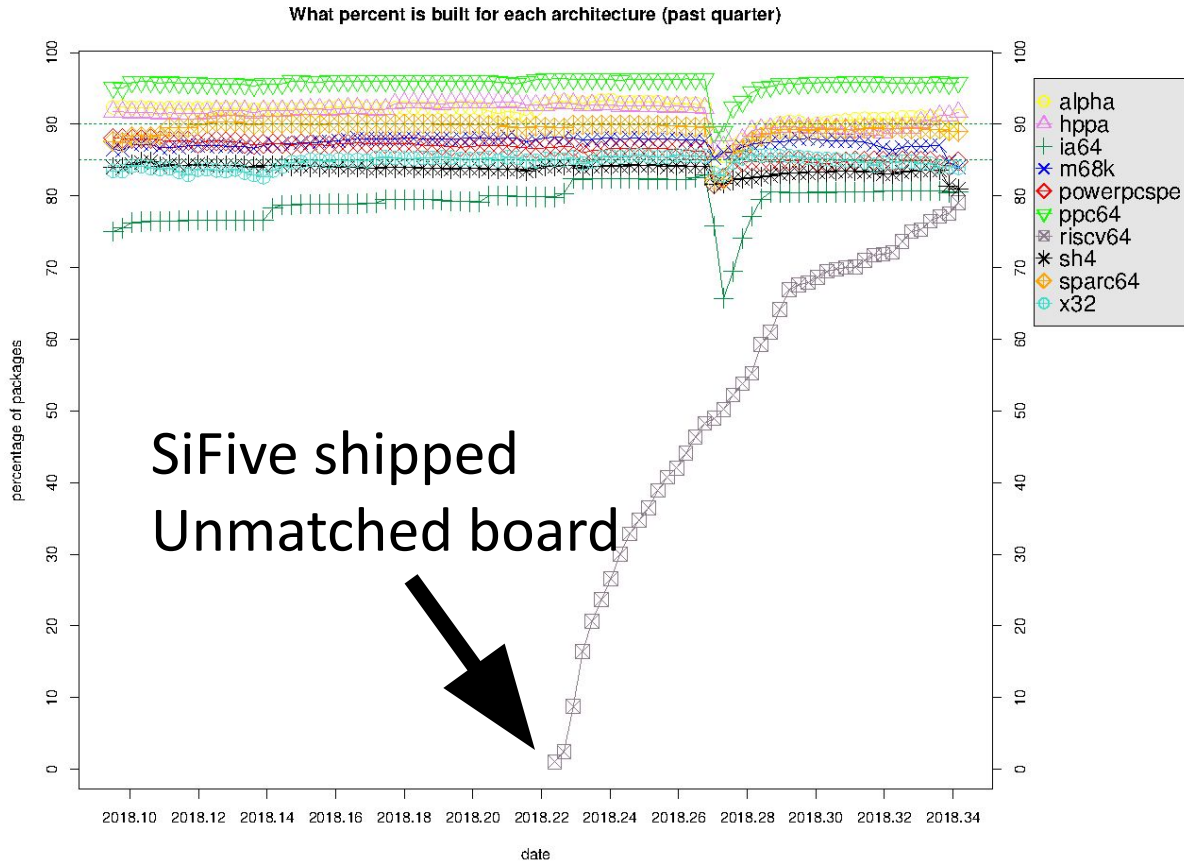
# RISC-V will have the best ecosystem

- Largest number of players
- All cores in system become RISC-V
- Software wants to run on the best hardware
  
- Hardware and software have been co-evolving rapidly
- Long-running silicon and core developments bearing fruit now
- As advantages and future become clearer, greater motivation to move to RISC-V
- Positive feedback on software ecosystem growth

# RISC-V ecosystem maturing rapidly

- Consider relatively advanced RISC-V software ecosystem despite very little development hardware to date
- New dev boards/products appearing en masse in next year or two
- E.g., Google announced Android support for RISC-V, Dec 2022

# Debian Port Progress



# Accelerating the Rich RISC-V Ecosystem

Security

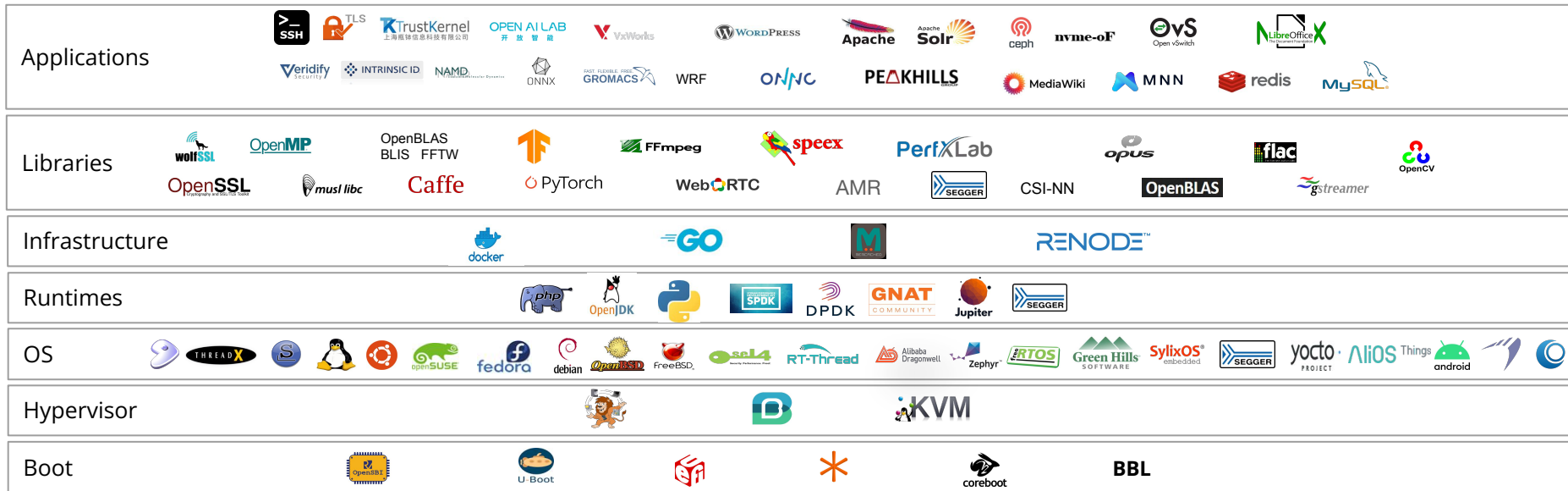
HPC

AI / ML

Cloud - Data Center - Storage - Networking

Consumer - IoT - Automotive

Mobile



**Design Tools + Compilers**

Buildbot, eclipse, gprof, Sparta, SEGGER, imperas, TinyEMU, EMU, SPIKE, SAIL, tvM, GDB, GCC, LLVM, Green Hills SOFTWARE, LAUTERBACH, IAR SYSTEMS, codeplay™

**Ecosystem Standards, upstream / support common tools**

ISA Extensions, Profiles, Platforms

Security model, IOMMU, Industry SIGs

**SAIL** Golden Model

**RISC-V ISA**

Architecture Tests

Attributes: Debuggable, Secure, Performant, Reliable/Serviceable/Diagnosable

**Implementation**

RTL | DV

**Design & Microarchitecture**

CHIPS ALLIANCE | lowRISC | OPENHW

Silicon Training Research | Soft IP Academia Services





# Android

- Google Support
- Google Requirements
  - Engagement with RISC-V
  - Likely in 2024
  - Much is underway
- Lifetime can be 10 years

# RT-Thread on RISC-V

## RV32

- HiFive1
- RV32M1\_VEG  
A
- HPM6750
- GD32VF103
- AB32VG1
- CH32V103
- CH32V208
- CH32V307
- CH569
- BL808
- ESP32C3

## RV64

- K210
- Allwinner D1
- Allwinner D1S
- QEUME/RISCV64  
VIRT

## RV-Core

- bumblebee
- QingKeV3
- QingKeV4
- E310
- cv32e40p
- Andes D45
- SMART-EVB for T-Head  
CPU E9xx Series
- PicoRV32

# Software Ecosystem Resources

- [Foundational Software Status](#) for each extensions
- Draft [spreadsheet](#) of software on RISC-V status (140+ being tracked)
  - Hired RVI Software Ecosystem Director. First task is a comprehensive one stop clearinghouse of RISC-V commercial and open source software status
- RISC-V Ecosystem [Landscape](#)
- RISC-V [Exchange](#) (100s)
- A new Linux Foundation Project named RISE to accelerate open source software development on RISC-V

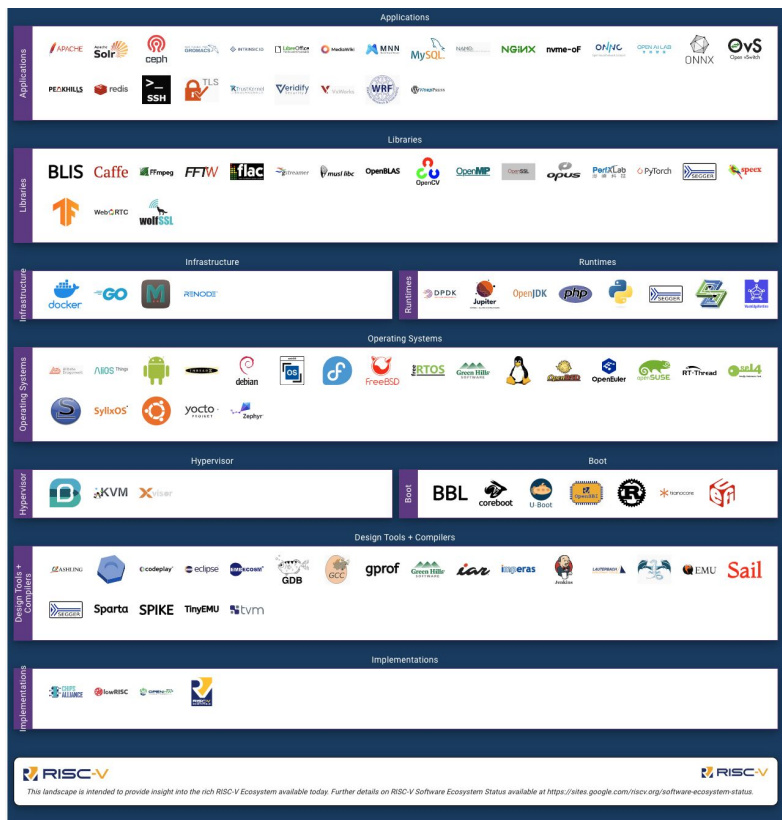
# Profiles with Key Ecosystem Status

extension/base name - best guess	ratification package name	description (what this does, in English)	IC	extensions included (subsets)	implies (and transitives)	incompatible (and transitive)	ratified (y/n)	ratified year (or expected) or future	MAJOR				ACT	SAIL	QEMU	SPIKE	GCC	LLVM	binutils	
									RV I20	RVA20 (64 only)	RVA22 (64 only)	RVA23 (64 only)								
									m - mandatory, mH - m if H is implemented, o - optional, n - non-profile options, p - part of an optional extension but not an optional extension itself											
									RV132 is only applicable to RVM and RVI profiles											
									Mode											
									U	S	U	S	U	S						
A	original	Atomics	unpriv	Zaamo, Zalrsc			y	2019	o	m	m	m	m	m	m	m	m	n	n	
C	original	Compressed instructions	priv				y	2019	o	m	m	m	m	m	m	m	m	y	y	
D	original	floating point, double-precision (implies F)	unpriv		F	Zdinx	y	2019	o	m	m	m	m	m	m	m	m	y	y	
F	original	floating point, single-precision	unpriv		Zicr	Zfinx	y	2019	o	m	m	m	m	m	m	m	m	y	y	
H	H	hypervisor	unpriv				y	2021	n	n	n	n	o	n	o		n/a	n/a		
M	original	multiply/divide	priv				y	2019	o	m	m	m	m	m	m	m	m	y	y	
N	N	user level interrupts	unpriv				n	future	n	n	n	n	n	n	n	n	n	n	n	
Q	original	floating point, quad-precision	priv				y	2019	n	n	n	n	n	n	n	n	n	n	n	
RV32E	RVE	integer base for RVE32	unpriv				y	2023	n	n	n	n	n	n	n	n	n	y	y	
RV32I	original	integer base for RVI32	unpriv				y	2019	m	n	n	n	n	n	n	n	n	n	n	
RV64E	RVE	integer base for RVE64	unpriv				y	2023	n	n	n	n	n	n	n	n	n	y	y	
RV64I	original	integer base for RVI64	unpriv				y	2019	m	m	m	m	m	m	m	m	m	n	n	
		only if H: For any hpmcounter that is not read-only zero, the																		

# Commercial & Open Source SW

Project Name	Source Code Location	mark's target	mark's categories	Project Area	Has it started work on RISC-V?	RISC-V Support Stage (the baseline is the x86_64 support when possible; supported means it has the base support for RISC-V, works, but there is still more work to be done; fully supported means out-of-box support for RISC-V)	riscv32	riscv64	oss or commercial	community-driven
LibreOffice	<a href="https://git.libreoffice.org/core/">https://git.libreoffice.org/core/</a>	user	app	Office Suite	1	supported	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Open Source	<input type="checkbox"/>
MediaWiki	<a href="https://github.com/wikimedia/mediawiki">https://github.com/wikimedia/mediawiki</a>	it	application	Collaboration	1	supported	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input checked="" type="checkbox"/>
WordPress	<a href="https://core.trac.wordpress.org/browser">https://core.trac.wordpress.org/browser</a>		application	Collaboration/Content Management	?	unknown	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input type="checkbox"/>
gcc	<a href="https://github.com/gcc-mirror/gcc">https://github.com/gcc-mirror/gcc</a>	developer	compiler	Toolchain	1	supported	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input type="checkbox"/>
GNU Mes	<a href="https://www.gnu.org/software/mes/">https://www.gnu.org/software/mes/</a>	developer	compiler	Bootstrap	1	in progress	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Open Source	<input checked="" type="checkbox"/>
GO	<a href="https://github.com/golang/go">https://github.com/golang/go</a>	developer	compiler	Toolchain	1	supported	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Open Source	<input type="checkbox"/>
Green Hills	?	developer	compiler	Operating System	1	supported	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Commercial	<input type="checkbox"/>
LLVM	<a href="https://github.com/llvm/llvm-project">https://github.com/llvm/llvm-project</a>	general development	compiler	Compiler	1	supported	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input type="checkbox"/>
Rust	<a href="https://github.com/rust-lang/rust">https://github.com/rust-lang/rust</a>		compiler	Language	1	supported	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input type="checkbox"/>
MariaDB	<a href="https://github.com/MariaDB/server">https://github.com/MariaDB/server</a>	infrastructure	database	Database	1	supported	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input checked="" type="checkbox"/>
memcached	<a href="https://github.com/memcached/memcached">https://github.com/memcached/memcached</a>	infrastructure	database	Storage	?	unknown	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input type="checkbox"/>
MongoDB	?		database	Database	?	unknown	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input checked="" type="checkbox"/>
MySQL	<a href="https://github.com/mysql">https://github.com/mysql</a>		database	Database	1	supported	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Open Source	<input type="checkbox"/>
Redis	<a href="https://github.com/redis/redis">https://github.com/redis/redis</a>		database	Database	1	supported	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Open Source	<input type="checkbox"/>
cryptoapi		security	library	library	?	unknown	<input type="checkbox"/>	<input type="checkbox"/>	Open Source	<input type="checkbox"/>
AIOS	<a href="https://github.com/OpenNucleus/AIOS-Things">https://github.com/OpenNucleus/AIOS-Things</a>	cloud	distro	Operating System	1	unknown	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Open Source	<input type="checkbox"/>

# Software Landscape



# RISC-V Exchange



About RISC-V | Membership | **RISC-V Exchange** | Technical | News & Events | Community | Search

## RISC-V Exchange

The RISC-V Exchange hosts the hardware, software, services, and learning offerings in the RISC-V community. Browse the list or search for an offering below.

SUBMIT AN ITEM

CONTACT US

Search Exchange...

Hardware  Cores  Software  Services  Learning

### Software

- Accelerated Libraries
- Accelerated Libraries, Linux, macOS
- Application Infrastructure
- Application Infrastructure, Simulators
- Bootloaders
- BSD Distro
- C Compilers and Libraries
- C compilers and libraries, Compilers and runtimes for other languages
- Cloud infrastructure
- Configuration
- Connectivity management
- Course materials
- Debugging
- Hypervisors
- RISC-V Cores

### CREATOR Simulator



**Organization:** UC3M  
CREATOR: didaCtic and geneRiC assEmbly progrAmming simulaTOR  
**Software Type:** Simulators

SOFTWARE

LEARN MORE

### emmtrix Parallel Studio



**Organization:** emmtrix Technologies GmbH  
emmtrix Parallel Studio allows the parallelization and code generation for different processors. With the support for the RISC-V architecture it provides capabilities to estimate the performance and generate C code for the CPU cores as well as for the vector extensions.

# Verification

- DV is done by implementers and DV providers
  - See [risc.org/exchange](https://risc.org/exchange) for a list of providers
- Implementations can be wildly different
- Open source implementations include full RTL and DV
- Compatibility is determined by passing basic architecture tests (supplied by RISC-V and depends on SAIL formal model for golden results) and self-attestation for OSs, DV, etc.





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**Change the  
World!**

# Questions

